9. Biasing BJTs

9.1 Transistor as an amplifier

A transistor can be use das an amplifier in three configurations

- Common base (CB)
- Common Emitter (CE)
- Common Collector (CC)

Because of the following reasons CE configuration is widely used

- High current gain
- High voltage and power gain
- Moderate output to input impedance ratio

Before discussing the transistor amplifier in details, it is important to note the following relations.

- The emitter current in a transistor is given by: $I_E = I_B + I_C$.
- The collector current $I_C = \beta I_B + I_{CEO} = \beta I_B + (\beta + 1) I_{CBO} \cong \beta I_B$
- The CB current amplification factor: $\alpha = \frac{I_C}{I_E}$
- The CE current amplification factor $\beta = \frac{I_C}{I_B}$
- The CC current amplification factor $\gamma = \frac{I_E}{I_B}$
- The relation between$\alpha, \beta \; and \; \gamma$: $\gamma = \frac{1}{1-\alpha} = \beta + 1$

The current and voltage in a transistor circuit includes both the value of dc (power supply) and ac (input signal). Hence following standard notations are used notations to distinguish ac and dc quantities.

$\boldsymbol{I_J}$ *denotes the dc quantities (eg:* V_{CC}, I_C, I_B, I_E, V_{BE}, V_{CE} *etc)*

$\boldsymbol{i_j}$ *denotes the ac quantities (eg:* v_{cc}, i_c, i_b, i_e, v_{be}, v_{ce} *etc)*

$\boldsymbol{i_J}$ *denotes ac and dc quantities (eg:* v_{CC}, i_C, i_B, i_E, v_{BE}, v_{CE} *etc)*

Figure 9.1 shows the basic amplifier circuit in CE configuration with an NPN transistor. In the circuit battery V_{BB} provides forward bias to E-B junction and battery V_{CC} provides reverse bias to CB junction. The magnitudes of these bias voltages are adjusted to operate transistor in active region. In this arrangement base is the input terminal and collector is the output terminal. The amplifier output is taken from the collector and ground.

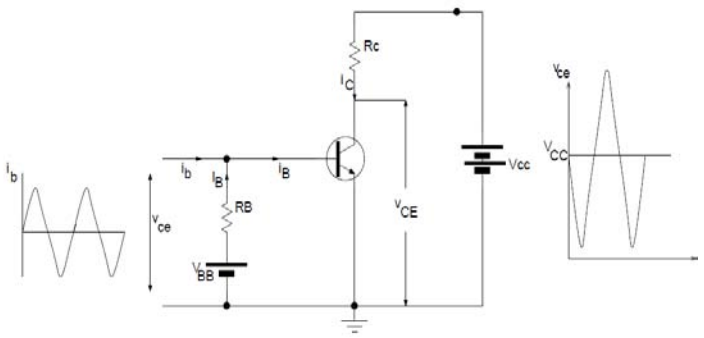

Fig 9.1 Transistor as an amplifier

When an input signal is applied in the E-B junction, the signal is super imposed in the dc voltage (V_{BB}), therefore during the positive half cycle of the input signal the forward bias increases, because it is already positive with respect to ground. This increase in forward bias increase the base current i_B, and hence i_C increases($i_C = \beta i_B$). During the negative half cycle of the input signal the forward bias decrease and hence the base current and in turn the collector current I_C decreases (β times)

Using KVL at the output section of the above circuit:

$$V_{CC} = v_{CE} + i_C R_C \quad (9.1)$$

Or, $$v_{CE} = V_{CC} - i_C R_C \quad (9.2)$$

where $i_C = I_C(dc) + i_c(ac)$, and $v_{CE} = V_{CE}(dc) + v_{ec}(ac)$

From the above equation it is clear that when the input current (i_b) =0, the collector to voltage will be V_{CC}. When the input current I_B increases, the output current i_C increases and hence the output voltage, V_{CE}, decreases (amplified in the –ve direction). Similarly when the input current i_b decreases, the output current i_C decreases and hence the output voltage, V_{CE}, increases (amplified in the +ve direction). That is the amplified output voltage across v_{CE} will be ***180^0 out of phase*** with the input current (I_B), or input voltage, v_{BE}.

9.2 DC Load line

In the amplifier circuit shown in figure 9.1, if no signal is applied to its input, the base current will be I_B (dc) only. At this state the transistor is said to be in quiescent state. At quiescent state V_{CC} sends a collector current I_C through the transistor. This current is called zero signal collector current. The magnitude of this current depends on the power supply V_{CC}, the load resistor R_L, and the collector to emitter voltage V_{CE} of the transistor. As I_C flows through the R_C and transistor, it will make voltage drop across the transistor.

Here, the voltage drop across $R_c = V_{Rc} = I_c R_c$ (9.3)

By applying KVL to the collector circuit, the voltage drop across the transistor is given by

$$\boldsymbol{V_{CE} = V_{CC} - I_c R_c} \quad (9.4)$$

Or $$\boldsymbol{I_C = -\frac{1}{R_c} V_{CE} + \frac{V_{CC}}{R_c}} \quad (9.5)$$

This equation is of the form $\boldsymbol{y = mx + c}$, which represents a straight line in the x-y graph. Similarly the above equation of I_C represents a straight line in the I_C-V_{CE} graph (i.e in the output characteristics of the transistor). The slope of the line **(m)=-1/R_C**. This straight line is called ***DC load line.*** Here the coordinates of this straight line in the I_C axis can be determined by setting V_{CE}=0.

That is by setting V_{CE}=0 in equation (9.5) we get $\boldsymbol{I_C = \frac{V_{CC}}{R_C}\Big|_{V_{CE}=0V}}$ (9.6)

Similarly the coordinates of load line in the V_{CE} axis can be determined by setting I_C=0, in the equation (9.5), that is, $\boldsymbol{V_{CE} = V_{CC}|_{I_C=0}}$ (9.7)

The two points obtained in the above steps are: **(V_{CC}, 0) and (0, V_{CC}/R_C).** By joining the two points we can draw the load line on the output characteristics of the transistor.

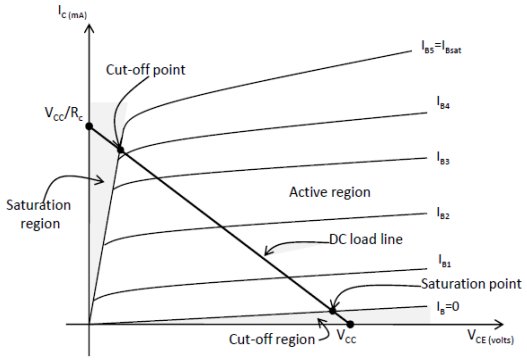

Fig 9.2 DC Load line

Cut-off point

The point of intersection of the load line and the output curve for $I_B=0$ is called cut-off point. The region below this point ($I_B<0$) on the load line is called cut-off region. At this region the E-B junction will not be forward bias.

Saturation Point

On the upper part of load line it intersects the curve $I_B=I_{B\ sat}$. This point of intersection is called saturation point. The region above this point on the load line is called saturation region. In this region collector junction will not be in the reverse bias. Hence the collector current will be almost saturated.

Active Region

The region between cut-off point and saturation point on the load line is called active region. In this region C-B junction will be in the reverse bias and E-B junction will be in forward bias.

9.3 Operating Point

As stated earlier at quiescent state, there will be a d.c. collector current through the transistor and is determined by V_{CC} and R_C. The point obtained by this value of I_C and V_{CE} at this time on the output characteristics is known as operating point. It is also called quiescent point, or simply 'Q' point.

The operating point is decided not only the characteristics of the transistor itself, but also a number of other factors such as V_{CC}, R_C, R_B, V_{BE} and V_{BB}. The exact location of the Q pint is on the dc load line is decided by the base current I_B and in turn I_B is decided by R_B, V_{BE} and V_{BB}. Applying KVL to the base circuit (fig 9.1),

$$V_{BB} = I_B R_B + V_{BE} \qquad (9.8)$$

Or

$$I_B = (V_{BB} - V_{BE})/R_B \qquad (9.9)$$

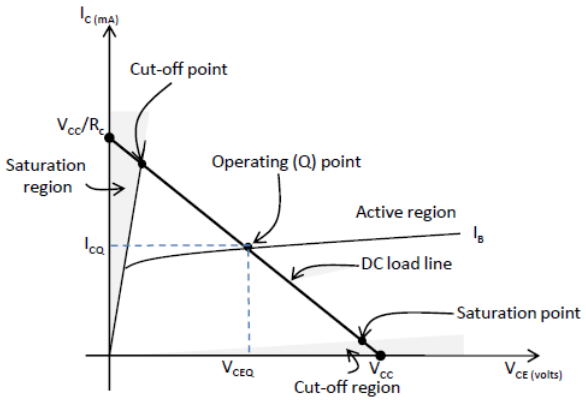

Fig 9.3 Operating point

9.4 Transistor Biasing and Stabilization

9.4.1 Selection of operating point

In order to get faithful amplification,

- The operating point must be well within the active region of the transistor.
- For useful operation,
  - The collector current I_C should not exceed the maximum current rating ($I_{C\,max}$).
  - The collector to emitter voltage V_{CE} should not exceed the value $V_{CE\,max}$.
    $I_{C\,max}$ and $V_{CE\,max}$ values of a transistor are prescribed by the manufacturer.
  - The maximum power rating P_{max}, determined by V_{Cmax} and IC_{max} values, should be considered.

There fore the working region of the transistor must be within the horizontal line I_{Cmax}, the vertical line through $V_{CE\ max}$, and the maximum power hyperbola ($P_{max} \propto I_{Cmax}^2$ or V_{CEmax}^2). This is indicated in the figure below. Hence the operating point should be within this active region, all time during the operation of amplifier.

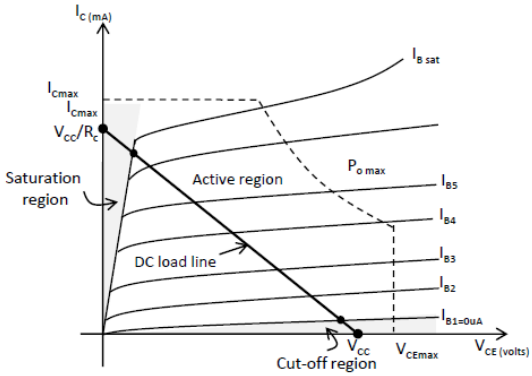

Fig 9.4 The Q point should be within the region bounded by $V_{CE\,max}$, I_{Cmax} and $P_{o\,max}$

After the dc conditions are established in the circuit, an ac signal voltage is applied to the input. Due to this voltage, the base current varies from instant to instant. A a result of this, the I_C and V_{CE} also vary with time. These variations current and voltages corresponding to a given of base current can be seen on the output characteristics of the transistor.

These variations are shown in figs below for the operating points A, B, and C respectively.

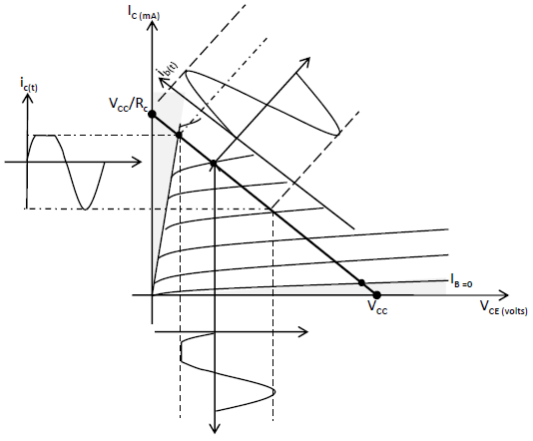

Fig 9.5 Operating region near saturation region gives clipping at the +ve and _ve peaks of Ic and Vce

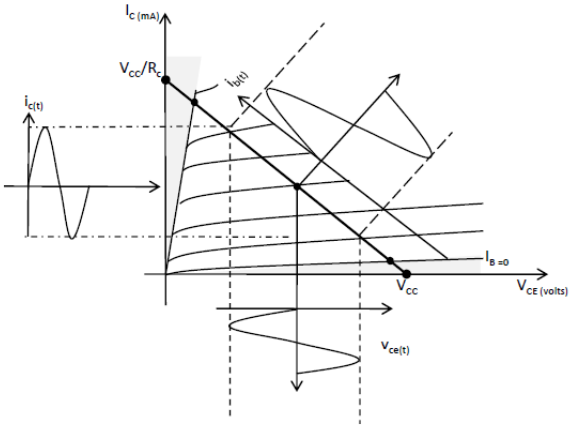

Fig 9.6 Operating point at the centre of active region is most suitable

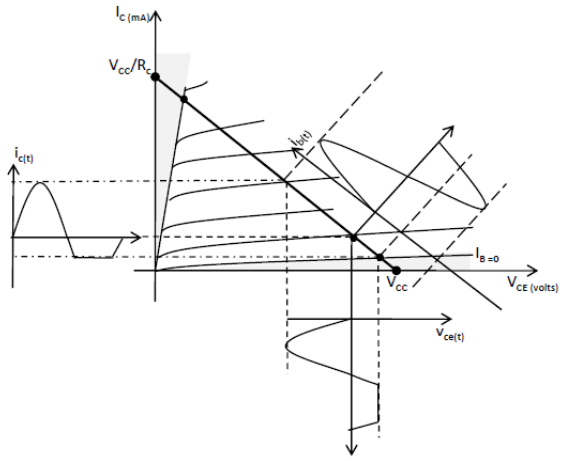

Fig9.7 Operating region near cut-off region gives clipping at the +ve and -ve peaks of Vce and Ic

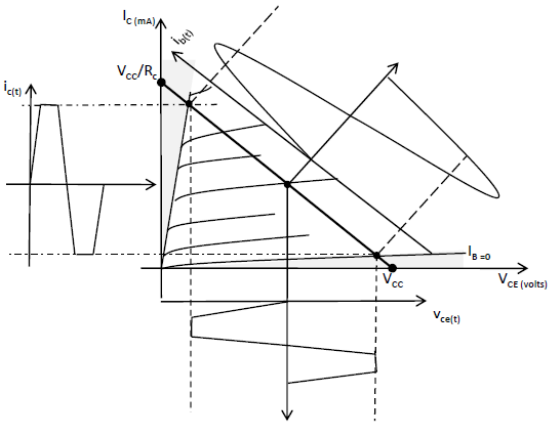

Fig 9.8 Distortion may result because of too large an input signal.

9.4.2 Bias Stabilization

Fixing a suitable operating point is not enough. It is very necessary to ensure that the operating point remains, where it is originally fixed. With continued use of an amplifier circuit, the operating point is found to shift in to undesirable region due to the following reasons:

- Change of parameters due to replacement of transistor
- Thermal variations

Change of parameters

The parameters transistor are varied even they are manufactured by the same firm and are of the same type. So when replacing one transistor in a circuit with anther of the same type and of the same manufacturer, the parameters such as β and V_{BE} of the new transistor will not be same as that of old one. This results in the shifting of operating point. Therefore the I_B must be allowed to change so as to maintain I_C and V_{CE} constant in spite of change in parameters such as β and V_{BE}.

Thermal Variation

The collector current of a transistor is given by the expression.

$$I_C = \beta I_B + I_{CEO} = \beta I_B + (\beta + 1) I_{CBO} \qquad (9.10)$$

The leakage current I_{CBO} *and* $_{CEO}$ are temperature dependent. It gets doubled for every 10^o raise in temperature. An increase in I_{CBO} due to temperature produces an increase in I_C of the transistor. This causes the collector junction temperature to rise, which in turn increase the value of I_{CEO}. This process being cumulative in nature may cause the junction temperature of the transistor to exceed its rated value, resulting the burn out of the transistor. This phenomenon is known as ***thermal run away.***

The process of making operating point independent of temperature changes and variations in transistor parameters is called ***stabilization***.

In order to keep operating point fixed, I_C and V_{CE} should be kept constant. There are two methods to keep I_C constant.

- ***Stabilization Technique:*** *Here resistive biasing circuits are used to allow* I_B *to vary to keep* I_C *relatively constant, with variation in* I_{CEO} (or I_{CO}), β *and* V_{BE}. *i.e.,* I_B *decreases if* I_{CO} *increase, to keep* I_C *constant. (see: biasing methods)*
- ***Compensation Technique:*** *In this method, temperature sensitive devices such as diodes, transistor, thermistors etc., which provide compensating voltage and currents to maintain the operating point constant are used.(see section: Bias Compensation)*

9.4.3 Stability Factors, $S(I_{CO})$, $S(V_{BE})$, and $S(\beta)$

A stability factor, S, is defined for each of the parameters affecting bias stability as listed below:

$$S(I_{CBO}) = \frac{\Delta I_c}{\Delta I_{CBO}}, \quad (9.11)$$

$$S(V_{BE}) = \frac{\Delta I_c}{\Delta V_{BE}}, \quad (9.12)$$

$$S(\beta) = \frac{\Delta I_c}{\Delta \beta}, \quad (9.13)$$

In each case, the delta symbol (Δ) signifies change in that quantity.

- Networks that are quite stable and relatively insensitive to temperature variations have low stability factors.
- The higher the stability factor, the more sensitive the network to variations in that parameter.

$$I_C = \beta I_B + (\beta + 1) I_{CBO}. \quad (9.14)$$

$$\Rightarrow \quad 1 = \beta \frac{dI_B}{dI_C} + \frac{(\beta+1)\, d(I_{CBO})}{dI_C}. \quad (9.15)$$

$$\Rightarrow \quad 1 = \beta \frac{dI_B}{dI_C} + \frac{(\beta+1)}{S} \qquad where\ S = \frac{dI_C}{dI_{CBO}}. \quad (9.16)$$

$$\Rightarrow \quad S = \frac{(\beta+1)}{1-\beta\frac{dI_B}{dI_C}}. \quad (9.17)$$

9.4.4 Biasing Circuits

Requirement of a biasing circuit

- Locate the operating point at the middle of the active region, under no signal condition, and keep the variation of operating point (when applying an input), within the active region only.
- Stabilize collector current against temperature variations.
- Make the operating point independent of transistor parameters.

Methods of Biasing

a. Base resistor (fixed) bias.
b. Feed back resistor bias.
c. Emitter resistor bias.
d. Voltage divider bias.

a. Fixed Bias

The fixed bias circuit is shown below. By taking KVL at the base-emitter loop, we get

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} \cong \frac{V_{CC}}{R_B} \quad (9.18)$$

In this equation V_{CC}, R_B, and V_{BE} are constant. That is I_B is fixed, once V_{CC} and R_B are selected; hence the name fixed bias. Once I_B is calculated, the collector current I_C can be calculated using: $I_C \cong \beta I_B, \quad constant$

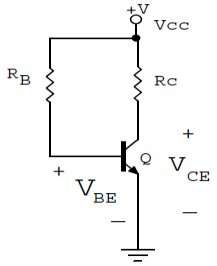

Fig 9.9 Fixed bias circuit

Similarly from the output section, using KVL,

$$V_{CC} = I_C R_C - V_{CE} \quad (9.19)$$

Or,

$$V_{CE} = V_{CC} + I_C R_C \quad (9.20)$$

This value of V_{CE} and calculated value of I_C provides the coordinates of Q point.

Stability factor $$S = \frac{(\beta+1)}{1-\beta\frac{dI_B}{dI_C}} = (\beta + 1) \quad (9.21)$$

It indicates that the value of S is very high, that is the circuit is more sensitive to variation in I_{CBO}. This is the main disadvantage of this circuit. This circuit also gives poor thermal stabilization.

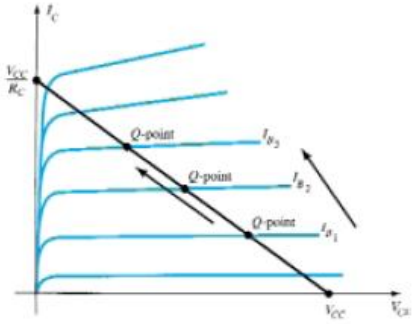

Fig9.10 Movement of Q point with increasing levels of I_B.

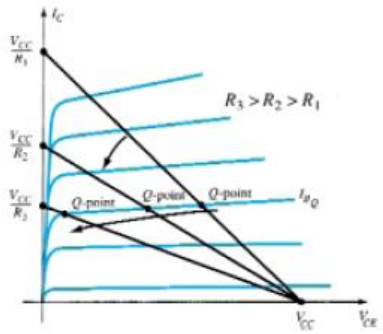

Fig 9.11 Effect of increasing levels of *RC* on the load line and *Q*-point.

b. Feedback Resistor (Voltage Feedback) Bias

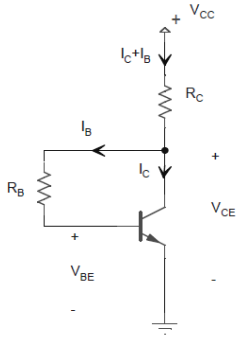

Fig 9.12 Feedback bias circuit

By analyzing the input section,

$$V_{CC} = (I_B + I_C)R_C + I_B R_B + V_{BE} \qquad (9.22)$$

Or, $$I_B = \frac{V_{CC} - I_C R_C - V_{BE}}{R_C + R_B} \qquad (9.23)$$

Similarly the KVL equation at the output gives,

$$V_{CE} = V_{CC} - I_C R_C \qquad (9.24)$$

Now, substituting the value of V_{CE} in the equation of I_B, gives,

$$I_B = \frac{V_{CE} - V_{BE}}{R_C + R_B} \qquad (9.25)$$

The collector current is then given by,

$$I_C = \beta I_B = \beta \frac{V_{CE} - V_{BE}}{R_C + R_B} \qquad (9.26)$$

This value of I_C and V_{CE} gives the operating point. Stability factor for feedback bias circuit is given by, the following equation.

$$S = (\beta + 1)\frac{1 + R_B/R_C}{(\beta + 1) + R_B/R_C} \rightarrow 1 \; for \; R_B/C \ll 1 \qquad (9.27)$$

This value of S ($= dI_C/dI_{CBO}$) indicates that, I_C will always increase at a rate equal to or grater than 1. The circuit also gives a negative voltage feed back from collector to base and hence the **gain reduces**. Feedback bias can provide thermal stabilization as indicated below, and hence the circuit can protect the transistor from thermal run away.

$$T(temperature) \uparrow \rightarrow I_{CBO} \uparrow \rightarrow I_{CEO} \uparrow \rightarrow \boldsymbol{I_C} \uparrow \rightarrow V_{CE} \downarrow \rightarrow I_B \downarrow \rightarrow \boldsymbol{I_C} \downarrow \qquad (9.28)$$

c.Emitter Bias

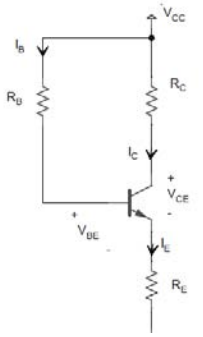

Fig9.13 Emitter bias circuit

Here an additional resistor R_E is added at the emitter of the transistor. The KVL at the input section gives, $$V_{CC} = I_B R_B + I_E R_E + V_{BE} \qquad (9.29)$$

We know, $$I_E = (\beta + 1)I_B \qquad (9.30)$$

Substituting this value of I_E and rearranging the previous equation will give,

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E} \qquad (9.31)$$

Now $$I_C = \beta I_B = \beta \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E}, \qquad (9.32)$$

This gives the coordinate I_C of the operating point.

Similarly applying KVL at the output give,

$$V_{CC} = I_C R_C + I_E R_E + V_{CE} = I_C(R_C + R_E) + V_{CE}, \qquad Since \; I_C \cong I_E \qquad (9.33)$$

$\therefore V_{CE} = V_{CC} - I_C(R_C + R_E)$, this gives the other coordinate V_{CE} of the Q point.

The stability factor, $S(I_{CBO})$ is given by,

$$S = (\beta + 1)\frac{1+R_B/R_E}{(\beta+1)+R_B/R_E} \rightarrow 1 \quad for\ R_B/R_E \ll 1 \qquad (9.34)$$

Similar to feedback bias arrangement, this value of S ($= dI_C/dI_{CBO}$) indicates that, I_C will always increase at a rate equal to or grater than 1. Or it depends on the values of R_B and R_E. The larger the value of R_E gives better stabilization (low S), but it will cause a large negative feed back at the input and hence the gain decreases. That is from the input loop it is clear that the base voltage,

$$V_B = V_{BE} + I_E R_E \text{ or } V_{BE} = V_B - I_E R_E \qquad (9.35)$$

So when the increase in R_E causes V_{BE} to decrease, and hence the output decreases. The emitter bias can provide thermal stability. When I_C increases, due to any increase in temperature, the drop $I_E R_E$ across R_E increase and hence the V_{BE} and I_B decreases. It causes I_C to decrease to its initial value.

d. Voltage Divider Bias

This is the most widely used method for providing biasing and stabilization for transistor. Fig shows the biasing circuit.

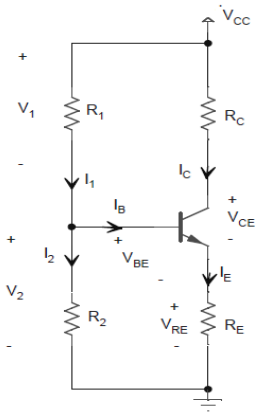

Fig 13 Voltage Dicider bias circuit

Analysis of input Section

The input section of the voltage-divider configuration can be represented by the network of Fig . The resistance R_i is the equivalent resistance between base and ground for the transistor with an emitter resistor R_E. The value of $R_i = (\beta+1)R_E$. And we are assuming $I_1 \approx I_2$ (since $R_i >> R_2$), using

$$V_{R2} = V_B \cong \frac{V_{cc} R_2}{R_1+R_2}. \qquad (9.36)$$

Also, $$V_B = V_{BE} + V_{RE} \qquad (9.37)$$

$$V_{BE} = V_B - V_{RE} \qquad (9.38)$$

Or, $$V_{RE} = V_B - V_{BE}$$

$$I_C \cong I_E = \frac{V_{RE}}{R_E} \qquad (9.39)$$

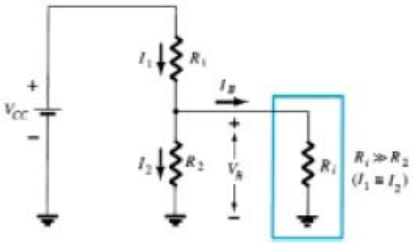

Fig 9.14 Approximate i/p equivalent circuit

Analysis of output Section

$$V_C = V_{CE} + V_E = V_{CC} - I_C R_C \qquad (9.40)$$

Or. $$V_{CE} = V_{CC} - I_C R_C - V_E, \qquad (9.41)$$

Or. $$V_{CE} = V_{CC} - I_C R_C - I_E R_E \qquad (9.42)$$

Or. $$V_{CE} = V_{CC} - I_C R_C - I_C R_E = V_{CC} - I_C(R_C + R_E) \qquad (9.43)$$

The value of and I_C, give the coordinate of operating point. It is to be noted that in the above discussion the value of β has never entered into any of the calculations. Hence change in β value will have no effect on the operating point. The circuit can provide thermal stability. When temperature, T increases, leakage current increases which causes I_C to rise. The increase in I_C causes the drop V_{RE} ($=I_E R_E$) to increase, hence the V_{BE} and then I_B decreases. Any decrease in I_B results in a decreased collector current, I_C. In this way voltage divider bias protect transistor from thermal run away. The stability factor S is given by,

$$S = \frac{\beta/R_E}{(\beta+1)+R_{TH}/R_E} \qquad where\ R_{TH} = R_1 || R_2 \qquad (9.44)$$

If we select $R_E >> R_{TH}$, the circuit will be more stable.

7.4.5 Bias Compensation

The collector to base bias circuit and self bias circuit are used for stability of I_C with variation in I_{CEO} V_{BE} and β. But we said that there is feed back from the output to the input. Hence the amplification will be reduced, even though the stability is improved.

a) Diode Compensation for V_{BE}.

A circuit utilizing the self bias stabilization technique and diode compensation is shown in fig 9.15. The diode is kept biased in the forward direction by the source V_{DD} and resistance R_D. if the diode is of the same material and type of the transistor, the voltage V_O across the diode will have the same temperature coefficient (-2.5mV/°C) as the base emitter voltage V_{BE}. If we write KVL around the base circuit, then

$$V_{cc} = I_B R_B + V_{BE} + I_E R_E - V_o, \qquad (9.45)$$

,we know that $I_C = \beta I_B + (\beta + 1) I_{CBO}$ *and* $I_E = I_C + I_B$

Therefore, $V_{cc} = \left[\frac{I_C - (\beta+1) I_{CBO}}{\beta}\right] R_B + V_{BE} + \left[I_C + \frac{I_C - (\beta+1) I_{CBO}}{\beta}\right] R_E - V_o \qquad (9.46)$

$$I_C = \frac{\beta [V_{cc} - (V_{BE} - V_O)] + (R_B + R_E)(\beta+1) I_{CBO}}{R_B + R_E (\beta+1)} \qquad (9.47)$$

Since V_{BE} tracks V_O (Q and D are of same material) with respect to temperature, it is clear fro the equation that I_C will be insensitive to variation in V_{BE}.

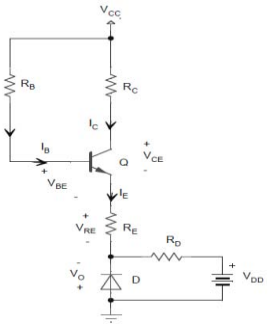

Fig 9.15 Stabilization by means of self bias and diode- compensation technique

b) Diode Compensation for I_{CO} ($=I_{CBO}$).

We know that changes of V_{BE} with temperature contribute significantly to changes in collector current of silicon transistor. On the other hand for germanium transistors, changes in I_{CO} with temperature will play the more important role in collector current stability. The diode compensation circuit shown in fig 9.16. offers stabilization against variations in I_{CO}, and is therefore useful for stabilizing germanium transistors.

If the diode and transistor are of the same type and material, the reverse saturation current I_O of the diode will increase with temperature at the same rate as the transistor collector saturation current I_{CO}. From the fig, we have,

$$I = \frac{V_{CC} - V_{BE}}{R_1} \cong \frac{V_{CC}}{R_1} = const \qquad (9.48)$$

Since the diode is reverse-biased by an amount $V_{BE} \approx 0.2V$ for germanium devices, it follows that the current through D is I_O.

The base current is $I_B = I - I_O$. Substituting this expression for I_B in the equation, we obtain

$$I_C = \beta I - \beta I_O + (1+\beta) I_{CO} \cong \beta I - \beta I_O + \beta I_{CO} = \beta I + (\beta I_{CO} - \beta I_O) \qquad (9.49)$$

If I_O of D and I_{CO} of Q track each other over the desired temperature range, then I_C remains essentially constant.

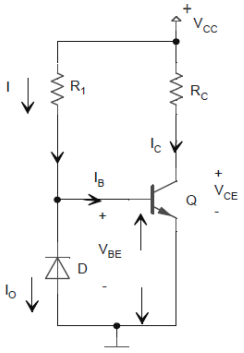

Fig 9.16 Diode- compensation or a germanium transistor.